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Model predictive control for pre-compensated voltage mode controlled DC–DC converters

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Abstract: This study introduces the use of model predictive control (MPC) to improve the performance of pre-compensated power supplies, and in particular of DC–DC converters, by dynamically modifying their output voltage reference. The importance of developing controllers for pre-compensated converters is twofold. First, the hierarchical structure is particularly useful when the primal controller is already coded, or hardware based, and cannot be changed. Second, the double-loop and, possible, multi-rate structure represents a computationally cheaper alternative to a direct MPC that would replace the primal controller and would require a much higher sampling frequency. In this study a MPC controller has been applied for the regulation of a pre-compensated synchronous DC–DC buck converter. The aim is to improve the performance of standard voltage mode control (VMC), without replacing the linear controller and without drastically affecting the computational burden. The algorithm has been tested both in simulation and experimentally, on commercially available hardware. The results show the performance improvement with respect to the standard VMC, as well as the feasibility of the proposed approach in an embedded platform. Tests with different primal controller tunings, and unknown varying loads, confirm the advantages of the method.

1 Introduction

In the very last years, the continuously increasing tightening of efficiency and performance requirements (ENERGY STAR®) enhanced several research branches in the control of power supplies [1–4]. Among them, model predictive control (MPC) saw a wide interest from both academy and industry [5–7]. MPC makes explicit use of the plant model to predict its future behavior, and it solves an optimal control problem at each sampling time [8]. The main aspects that favoured the interest of MPC in this field are the intuitive design and tuning of the controller, the enhanced performance and the availability of relatively accurate models for electrical devices [9–11]. Such highly requested features come at the cost of cumbersome online calculations, which have limited the spread of the method in fast-sampled systems. For these reasons, researchers have been encouraged in looking into efficient solutions for embedded MPC implementations [12], instead of using powerful embedded boards, such as field programmable arrays, that could not be available for such systems [13, 14]. Moreover, the very recent complexity certification of quadratic programming (QP) solvers is a step forward into safe implementation of embedded MPC [12]. When dealing with transistors-based devices, the literature splits into two branches. *Continuous Control Set* (CCS)-MPC takes control actions into a continuous set, which is usually the duty cycle of the pulse width modulation (PWM). *Finite control set* (FCS)-MPC exploits the discrete nature of power converters and takes action in a discrete control set namely the finite combinations of predicted switches' states [1, 10]. To deal with the computational load, explicit MPC is the preferred solution for CCS-MPC. It pre-solves the optimisation problem through multiparametric quadratic programming (mpQP), and the implemented controller turns to be a piece wise affine function of parameters, easy to be applied online [15]. Explicit MPC has already been successfully used for power converters control [2, 16, 17]. However, it becomes impractical when the number of inputs or the prediction horizon is not small enough, due to the high-memory requirements. On the other hand, several algorithms have been proposed to efficiently implement FCS-MPC, and to achieve long prediction horizons [10, 18]. The performances of CCS and FCS-MPC have been recently compared [19, 20]. FCS-MPC usually provides a faster response time than CCS-MPC. However, CCS-MPC decouples the switching frequency from the controller sampling time, and it operates the converter at a fixed frequency. For these reasons CCS-MPC is more often preferred in industrial applications.

The aim of this paper is to investigate CCS-MPC for pre-compensated DC–DC converters. Following the idea of the reference governor (RG), this paper presents the design of an MPC loop that regulates a DC–DC converter while manipulating the reference of the actual primal controller [21–25]. Several engineering fields have already experimented the use of RG, such as automotive and robotics [26, 27]. However, the focus of the current research on power electronics' control algorithms, is almost completely based on replacing the standard controller. Only few recent attempts can be found where the modification of the reference is used to improve the transient response of standard controllers [28, 29]. Power conversion seems to be a field where the control of pre-compensated systems could find an important role. Indeed, very often there is no possibility to change the native controller, which is hard coded or even hardware-based [30]. The designer could also have the necessity to retain the primal controller due to stability and robustness certification [31]. Furthermore a double loop, multi-rate, control structure would permit to exploit the benefits of MPC with a slower sampling frequency, improving the feasibility of CCS-MPC in such fast sampling and computationally cheap systems. A preliminary study of the topic has been recently proposed by the authors in [32]. The controller designed here aims to regulate the reference of a voltage mode control (VMC) algorithm, that steers the output voltage of a synchronous buck DC–DC converter. Synchronous rectification is particularly attractive for efficiency optimisation with respect to the standard asynchronous rectification, and VMC is the simplest control technique for PWM converters, regulating the duty cycle of the gating PWM signal to track a desired output voltage [33, 34]. VMC is implemented with a linear PI regulator. In the proposed work, the implemented MPC controller regulates the voltage reference solving an unconstrained optimal control problem at each sampling time. Unconstrained formulation is very cheap in terms of memory and computational load, and does not require neither an embedded solver or an explicit solution or a powerful board. The

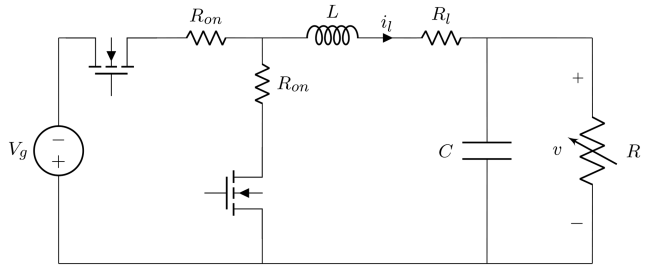

Fig. 1 *Electrical schematic of the synchronous DC–DC buck converter*

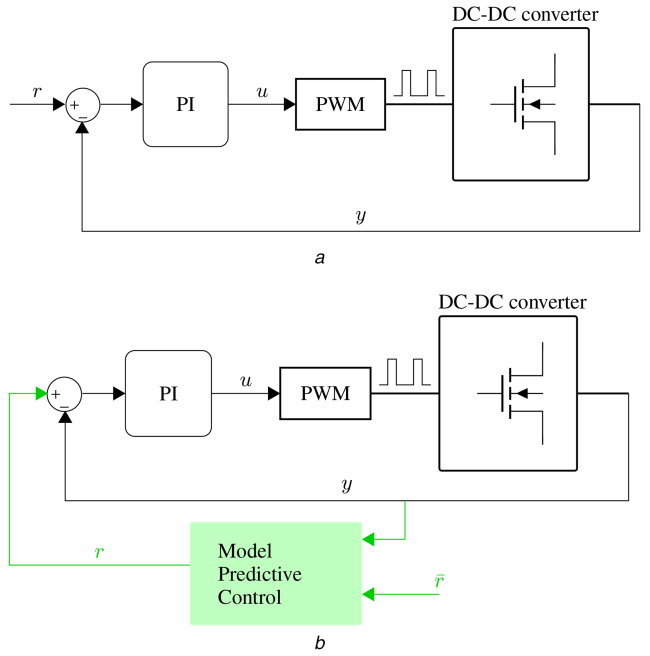

Fig. 2 *Block scheme of the standard VMC 2a, and the MPC applied to the pre-compensated system 2b. The added part is highlighted in green, the other remains unchanged*
(a) Standard VMC, ***(b)*** Proposed MPC-VMC

results show that, in the considered application, adding constraints is not necessary. However, a constrained formulation is a possible extension of the work, in particular considering current limits. Compared to the method in [28], the algorithm does not need any current sensor, leaving unaltered the hardware and software setup of the standard VMC. Furthermore, the use of MPC framework allows to exploit its intuitive tuning process, and opens the door to future input/output constrained implementations. Experimental tests on commercially available hardware from Texas Instruments© are presented. The results show that the proposed technique, that we refer to as MPC-VMC, is able to deeply improve the control response without demanding high currents and without changing the original controller. The feasibility of the approach is also demonstrated by implementing the algorithm on a low-power board, which is commonly used in power electronics and electrical motor control.

The paper is organised as follows. Section 2 introduces the converter model and summarises briefly the VMC scheme. Section 3 details the MPC scheme and and its implementation. Section 4 collects the simulation and experimental results, with a synchronous buck converter. Finally Section 5 concludes the paper.

2 DC–DC buck converter

In this section the mathematical model of the synchronous buck converter is obtained and the standard VMC is presented. The electrical schematic of the converter is shown in Fig. 1, where the main parasitic components that affects the mathematical model are represented. These are well known concepts and only the basics are provided for the ease of the reader. Detailed information can be easily found in the literature, e.g. in [34].

2.1 Mathematical model

DC–DC converters are switching systems due to the discrete input that assumes values in the set $\{0, 1\}$. This input corresponds to the on/off state of the switch. Although discrete actuation is a possible alternative, PWM converters are usually preferred in industrial applications. The main reason is the fixed switching frequency provided by the modulator which reduces the stress of the components. In addition, this permits to decouple switching and control frequencies, guaranteeing at the same time good ripple reduction and satisfactory sampling time. The model of PWM converters are averaged continuous model over a switching period [34]. For the DC–DC buck converter considered in this paper, the averaged model is:

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{1a}$$

$$y(t) = Cx(t) \tag{1b}$$

with $x \in \mathbb{R}^{n_x}$, $u \in \mathbb{R}^{n_u}$, $y \in \mathbb{R}^{n_y}$, and

$$A = \begin{bmatrix} -\dfrac{R_l + R_{on}}{L} & -\dfrac{1}{L} \\ \dfrac{1}{C} & -\dfrac{1}{CR} \end{bmatrix}, \quad B = \begin{bmatrix} \dfrac{V_g}{L} \\ 0 \end{bmatrix}, \quad C = [0 \quad 1]. \tag{2}$$

The states $x(t) = [i_l(t) \quad v(t)]'$ are the inductor current and the output voltage, respectively, whereas the input $u(t) = d(t)$ is the duty cycle of the PWM and gets values in the range $\mathbb{R}_{[0,1]}$. L and C are the inductor and capacitor values, R_l and R_{on} the parasitic components of the inductor and switch, V_g is the input voltage, and R is the supplied load.

Synchronous converters are usually controlled with a single input, with a master-slave technique that drives the two switches [34]. In buck converters the primary switch is high-side, and directly driven by the PWM signal. The second transistor is low-side, and actuated by a complementary signal.

2.2 Voltage mode control

Voltage-based control must guarantee the regulation of the output voltage at the desired value. The most widely used controllers are VMC and current mode control (CMC), and nowadays they are considered a technology [34, 35]. The first has a single loop with voltage feedback, the second presents a cascaded structure with inner current and outer voltage control loops. CMC exploits the faster dynamics of the current to provide a responsive control and over current protection, however it needs a current sensor which brings extra cost, space and susceptibility to noise [35]. For these reasons, VMC is preferred in some applications for its simplicity. Nonetheless VMC and CMC are still subject of research for performance improvements [2, 36]. However, standard linear control is the first choice for consumer electronics, and improvements in this field are not the aim of this work. We implemented the standard VMC, with a linear proportional integral (PI) regulator [34]. The block scheme of the controller is depicted in Fig. 2*a*. The parameters of the controller are tuned with small-signals modeling, see e.g. [37]. Bandwidth and stability margins are usually considered to obtain a satisfactory controller. As a rule of thumb, a controller that exhibits a gain margin of about 10 dB and a phase margin greater than 45° is desirable [34, 37]. The linear controller derived in this paper has been obtained following this general rule of thumb.

3 Controller design

Standard MPC solves a finite-horizon, optimal control problem based on a linear prediction model of the process [8, 15]. The interest in this technique is growing in power supplies. The ease in handling multivariable systems, imposing input/output constraints and the intuitive design process are some of the key factors that contributed to this interest [1, 18]. Indeed, the wide literature on the topic assessed MPC as one of the leading technology for the

future of power electronics control [6]. However, two motivations can prevent the direct use of the MPC as a primal controller:

• a primal controller is already embedded into the physical system, either software or hardware, and cannot be modified;
• the dynamics of the system are too fast and a primal MPC is not feasible, thus a double, multi-rate, loop is preferred.

This paper addresses those problem, and presents the design of an MPC regulator for a pre-compensated power converter, following the idea of RG [21, 23]. The aim is to enhance the performance of the primal controller, without substituting it. It is assumed that a primal controller, namely the VMC discussed in Section 2.2 is already available and able to control the system properly.

3.1 Closed-loop model

To design the MPC controller, the mathematical model of the pre-compensated closed-loop system must be known, and it is derived in the following. The purpose of this section is to remain as general as possible, thus the controller derivation is carried out for a PID regulator, even if PI controllers usually guarantee satisfactory performance for DC–DC converters.

The discrete-time linear time invariant (LTI) model of the system is directly obtained from (1) and (2), such as

$$x(k+1) = A_{\mathrm{d}}x(k) + B_{\mathrm{d}}u(k) \tag{3a}$$

$$y(k) = C_{\mathrm{d}}x(k), \tag{3b}$$

where $k \in \mathbb{N}$ is the discrete-time index, $A_{\mathrm{d}} = e^{AT_{\mathrm{s}}}$, $B_{\mathrm{d}} = \int_0^{T_{\mathrm{s}}} e^{A\tau}\,\mathrm{d}\tau B$, and $C_{\mathrm{d}} = C$, are the discrete-time state-space matrices. The primal controller function is assumed to be equal to

$$u(k) = \left(K_{\mathrm{p}} + K_{\mathrm{i}}T_{\mathrm{s}}\frac{z}{z-1} + K_{\mathrm{d}}\frac{\delta}{1+\delta T_{\mathrm{s}}(z/(z-1))}\right)e(k) \tag{4}$$

where K_{p}, K_{i} and K_{d} are the proportional, integral and derivative gains, T_{s} is the sampling frequency, $\delta = 1/t_f$ is the derivative filtering term and $e(k)$ is the tracking error. The discrete-time state-space model of (4) is:

$$x_{\mathrm{p}}(k+1) = \underbrace{\begin{bmatrix}1 & 0\\ 0 & \alpha\end{bmatrix}}_{A_{\mathrm{p}}}x_{\mathrm{p}}(k) + \underbrace{\begin{bmatrix}\tilde{K}_i\\ -\tilde{K}_{\mathrm{d}}(1-\alpha)\end{bmatrix}}_{B_{\mathrm{p}}}u_{\mathrm{p}}(k) \tag{5a}$$

$$y_{\mathrm{p}}(k) = \underbrace{\begin{bmatrix}1 & 1\end{bmatrix}}_{C_{\mathrm{p}}}x_{\mathrm{p}}(k) + \underbrace{\begin{bmatrix}K_{\mathrm{p}} + \tilde{K}_i + \tilde{K}_{\mathrm{d}}\end{bmatrix}}_{D_{\mathrm{p}}}u_{\mathrm{p}}(k) \tag{5b}$$

where the subscript p stands for *primal controller* and

$$\tilde{K}_i = K_{\mathrm{i}}T_{\mathrm{s}} \tag{6a}$$

$$\tilde{K}_{\mathrm{d}} = \frac{K_{\mathrm{d}}}{T_{\mathrm{s}} + t_f} \tag{6b}$$

$$\alpha = \frac{t_f}{t_f + T_{\mathrm{s}}}. \tag{6c}$$

One can trivially verify that $y_{\mathrm{p}}(k) \equiv u(k)$ and $e(k) \equiv u_{\mathrm{p}}(k) \equiv r(k) - y(k)$ where $r(k) \in \mathbb{R}^{n_y}$ is the reference signal for the controlled system, that is the output voltage reference.

Let $y_c(k) \equiv y(k)$ be the output of the extended system, and consider the extended state vector $x_c(k) \in \mathbb{R}^{n_{x_c}}$ defined as

$$x_c(k) = \begin{bmatrix}x_{\mathrm{p}}(k)\\ x(k)\end{bmatrix}. \tag{7}$$

The extended open-loop system is therefore equal to

$$x_c(k+1) = \underbrace{\begin{bmatrix}A_{\mathrm{p}} & 0\\ B_{\mathrm{d}}C_{\mathrm{p}} & A_{\mathrm{d}}\end{bmatrix}}_{A_c}x_c(k) + \underbrace{\begin{bmatrix}B_{\mathrm{p}}\\ B_{\mathrm{d}}D_{\mathrm{p}}\end{bmatrix}}_{B_c}u_{\mathrm{p}}(k) \tag{8a}$$

$$y_c(k) = \underbrace{\begin{bmatrix}D_{\mathrm{d}}C_{\mathrm{p}} & C_{\mathrm{d}}\end{bmatrix}}_{C_c}x_c(k) + \underbrace{\begin{bmatrix}D_{\mathrm{d}}D_{\mathrm{p}}\end{bmatrix}}_{D_c}u_{\mathrm{p}}(k), \tag{8b}$$

with the tracking error $e(k) \equiv u_{\mathrm{p}}(k)$ as its only input. The closed-loop model derived from (8) is

$$x_c(k+1) = A_f x_c(k) + B_f r(k) \tag{9a}$$

$$y_c(k) = C_f x_c(k) + D_f r(k) \tag{9b}$$

where, by setting $d \triangleq (D_c + 1)^{-1}$, the following equations hold

$$A_f = A_c - B_c C_c d \tag{10a}$$

$$B_f = B_c - B_c D_c d \tag{10b}$$

$$C_f = C_c d \tag{10c}$$

$$D_f = D_c d\,. \tag{10d}$$

Model (9), with matrices defined as in (10), represents the closed-loop system of an LTI system controlled by a linear PID regulator. However, it is a common practice to use simple PI controllers for DC–DC converters as they are proven to give satisfactory performance for such systems [34]. This holds true also for the experimental results presented in this work, that is $K_{\mathrm{d}} = 0$ in (4). With a standard controller the provided set-point and the reference to the primal controller are the same, namely $r = \bar{r}$. With MPC-VMC, the set-point is $\bar{r}$ and the dynamical reference to the primal controller is $r(k)$, see Figs. 2*a* and *b*.

3.2 Model predictive control

At each sampling time linear MPC solves a finite-horizon, optimal control problem based on a prediction model of the controlled process and an estimation of its current state, provided by a Kalman filter. For the state of the art in MPC, the reader is referred to [8]. In embedded MPC, the time required to solve the optimization problem is not negligible with respect to the sampling interval. Therefore, for a correct synchronization, the input computed by MPC is applied to the system with one-step delay. Consequently MPC regulates the following system:

$$x_c(k+1) = A_f^{\eta}x_c(k) + B_f^{\eta}\mathring{r}(k-1) \tag{11a}$$

$$y_c(k) = C_f^{\eta}x_c(k) + D_f^{\eta}\mathring{r}(k-1) \tag{11b}$$

with $\mathring{r}(k-1) = r(k)$, and A_f^{η}, B_f^{η}, C_f^{η}, D_f^{η} the state-space matrices of the discrete-time system (9) down sampled at $T_{\mathrm{s}}^{\eta} = \eta T_{\mathrm{s}}$, with $\eta \geq 1$. This formulation allows the MPC controller to eventually run at slower frequency with respect to the primal controller, for computational load reasons. In this paper a quadratic cost is minimised subject to the linear equality constraints representing the model dynamics, such that:

$$\min_{\Delta\mathring{r}}\ \sum_{i=1}^{N_{\mathrm{p}}} \| Q(y_{c,k+i|k} - \bar{r}(k)) \|_2^2 + \sum_{j=0}^{N_u-1} \| R\Delta\mathring{r}_{k+j|k} \|_2^2 \tag{12a}$$

$$\text{s.t.}\ \ x_{c,k|k} = \hat{x}_{c,k|k-1}, \tag{12b}$$

$$x_{c,k+i+1|k} = A_f^{\eta}x_{c,k+i|k} + B_f^{\eta}\mathring{r}_{k+i|k}, \tag{12c}$$

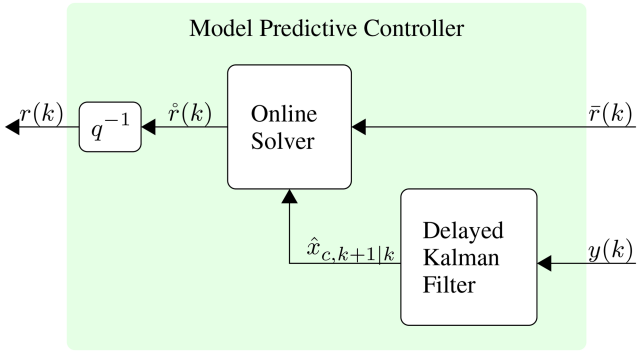

Fig. 3 *Block scheme of the MPC*

Table 1 Hardware and software specifications for simulation and experimental tests

Parameter	Symbol	Value	Units
DC–DC buck converter			
input voltage range		4.75–14	V
output voltage range		0.7–3.6	V
switching frequency		400	kHz
inductance	L	0.9	μH
inductance parasitic resistance	R_l	2.2	m Ω
capacity	C	470	μF
transistor parasitic resistance	R_{on}	3.6	m Ω
load resistance	R	1	Ω
Controllers' Parameters			
primal control frequency	T_{s}	400	kHz
MPC control frequency	T_s^{η}	100	kHz
proportional gain	K_{p}	0.0195	
integral gain	K_{i}	350	
prediction horizon	N_{p}	10	
control horizon	N_u	5	
measured output weight	Q	5	
manipulated variable rate weight	R	0.1	

$$y_{c,k+i+1|k} = C_f^{\eta} x_{c,k+i+1|k} + D_f^{\eta} \mathring{r}_{k+i|k}, \tag{12d}$$

$$\Delta \mathring{r}_{k+N_u+j|k} = 0, \tag{12e}$$

$$i = 0, 1, \ldots, N_{\text{p}} - 1, \tag{12f}$$

$$j = 0, 1, \ldots, N_{\text{p}} - N_u - 1, \tag{12g}$$

where N_{p} is the prediction horizon, N_u is the control horizon, Q and R denote the weight matrices, $x_{c,k+i|k}$ is the prediction of x at time $k+i$ based on information available at time k, $\Delta \mathring{r}_{k+i|k} = \mathring{r}_{k+i|k} - \mathring{r}_{k+i-1|k}$ is the vector of input increments and $\hat{x}_c$ is the state estimation. To cope with the input delay, the open loop optimal control problem is initialised at each time step, with a predicted state estimation, computed by the following Kalman filter:

$$\hat{x}_{c,k+1|k} = (A_f^{\eta} - LC_f^{\eta})\hat{x}_{c,k|k-1} + B_f^{\eta} - LD_f^{\eta} \mathring{r}_{k-1} + Ly_k \tag{13}$$

where L is the Kalman gain. The Kalman filter guarantees also the mitigation of the noise. Fig. 3 shows the block scheme of the proposed MPC, where q^{-1} represents the one-step delay operator.

Problem (12) can be cast into the parametric unconstrained QP problem

$$\min_z \; \frac{1}{2} z^{\text{T}} H z + p^{\text{T}}(k) F^{\text{T}} z \tag{14}$$

where $z \in \mathbb{R}^{n_z}$ and $p(k) \in \mathbb{R}^{n_{\text{p}}}$ are the vectors of optimization variables and time-varying affine parameters, respectively. Note that in this formulation the optimisation variables correspond to the inputs increments of the PWM duty-cycle that drives the transistors. The parameters' vector for the control of the closed-loop buck converter is

$$p(k) = [\mathring{r}(k-1) \;\; \hat{x}_c(k) \;\; \bar{r}(k)]^{\text{T}}. \tag{15}$$

The solution z^* of the problem (14) is analytic and equal to

$$z^* = H^{-1} F p(k). \tag{16}$$

Being z^* the optimal sequence of input increments, only the first n_{u} components are considered and applied to the system. Thus, the solution of the unconstrained MPC problem reduces to a matrix vector product, where the first n_{u} rows of $H^{-1}F$ are computed offline and stored. However, for such high-speed problems as power converters, even the unconstrained solution does not represent a negligible cost for low-power embedded boards. The advantage of the double, multi-rate, loop is the possibility to run MPC in a slower task respect to the primal controller.

Considering both the solution of problem (14), and the computation of the estimated state (13), the complexity c of the control algorithm can be explicitly computed as

$$c = (2n_{\text{p}} - 1)n_{\text{u}} + (2n_y + 2n_{\text{u}} + 2n_{x_c} - 1)n_{x_c}. \tag{17}$$

4 Simulation and experimental results

The proposed control technique was tested both in a simulation environment, and experimentally. The PTD08A010WAD 10A synchronous buck converter has been used [38] in conjunction with a Delfino F28335 digital power control module, commonly used in power systems, running VMC and MPC-VMC algorithms. They are commercially available, by Texas Instruments©, and the buck converter main parameters are listed in Table 1. The control scenario consists into supplying a 1 Ω–4 W load with 1 and 2 V DC voltage. The input supply voltage is 9 V, and the switching frequency is set to 400 kHz. The simulation tests have been carried out on PSIM® software (by Powersim Inc), which allows for the simulation of both analog and digital components, and control algorithms. The electrical model of PTD08A010WAD, based on [38], is available in PSIM® demo library.

The controller tuning has been reported in Table 1. The primal controller, running at 400 kHz has been tuned with a standard methodology based on the transfer functions derived from the model (1), (2). The PI gains have been tuned in order to meet the stability margins as mentioned before, namely a gain margin of 10 dB and a phase margin of more than 45° [37]. The MPC applied to the pre-compensated runs with a sampling frequency of 100 kHz, in order to demonstrate that notable control improvements are obtained applied the proposed algorithm even when the reference is changed slower with respect to the primal control frequency.

Two different tests have been proposed. The first consists in a positive step in the reference voltage from 1 to 2 V. The second one consists in a negative step from 2 to 1 V. For both tests the MPC-VMC performance are compared with standard VMC. Obviously, for both VMC and MPC-VMC, the primal controller is the same, namely a PI regulator with the same design parameters. Figs. 4 and 5 show the comparison between VMC and MPC-VMC during the transients of a positive and a negative step in the output voltage reference, respectively. Both the inductor current and the output voltage are shown, as well as the dynamically modified reference for the MPC-VMC algorithm. The results demonstrate the improvements in control performance, when applying MPC-VMC, regarding the rise time τ_{r} and the settling time τ_{s}. Indeed, during the positive step, MPC-VMC exhibits a reduction of 43.06 and 41.76% of the rise time and the settling time, respectively. Whereas, during the negative step the rise time and the settling time are reduced by 42.09 and 40.89%, respectively.

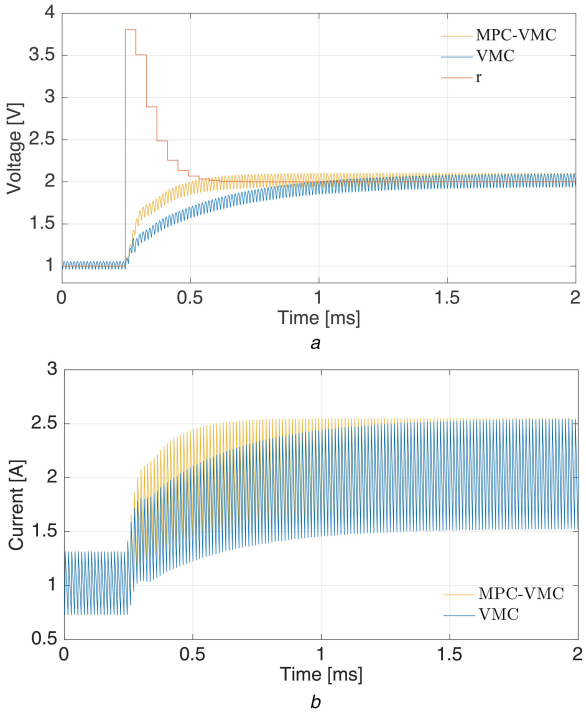

Fig. 4 *Simulation results, with an increasing output voltage step. Comparison between standard VMC and and MPC-VMC. From top to bottom: the output voltage, together with the modified reference value; the inductor current*

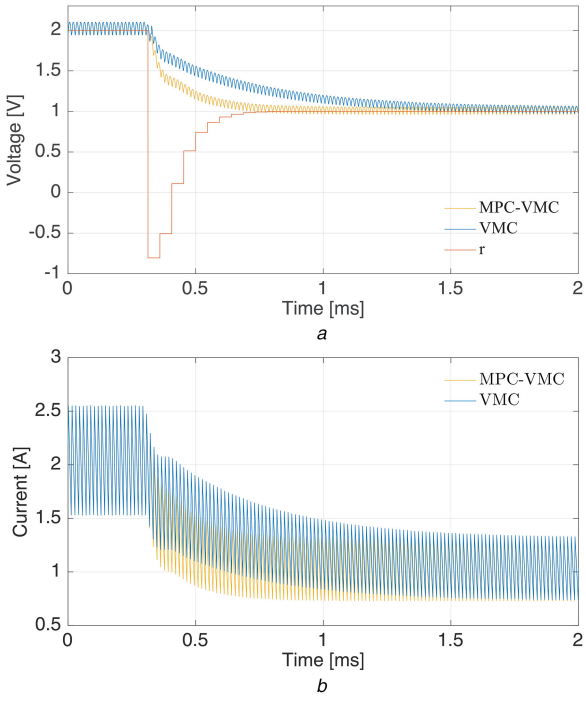

Fig. 5 *Simulation results, with a decreasing output voltage step. Comparison between standard VMC and and MPC-VMC. From top to bottom: the output voltage, together with the modified reference value; the inductor current*

To verify the sensitivity to parameters uncertainties, the two algorithms have been tested under load variations. The tuning of the two controllers is the same of the above experiment, namely Table 1, but the load value has been changed from a minimum of 0.2 Ω to a maximum of 2 Ω. Table 2 collects the results when comparing the standard VMC and MPC-VMC in several perturbed scenarios, during a positive voltage reference step. It is evident that MPC-VMC is always able to improve the performance, even when the load R is significantly changed respect to the value where the

Table 2 Performance comparison of VMC and MPC-VMC under unknown load variations for a positive reference step

Load	VMC		MPC-VMC	
R, Ω	τ_r, ms	τ_s, ms	τ_r, ms	τ_s, ms
0.2	0.51	0.65	**0.31**	**0.39**
0.4	0.61	0.77	**0.35**	**0.45**
0.6	0.67	0.84	**0.38**	**0.49**
0.8	0.70	0.88	**0.40**	**0.51**
1	0.72	0.91	**0.41**	**0.53**
1.2	0.73	0.93	**0.42**	**0.54**
1.4	0.74	0.93	**0.42**	**0.55**
1.6	0.75	0.94	**0.43**	**0.56**
1.8	0.76	0.96	**0.44**	**0.56**
2	0.77	0.97	**0.44**	**0.57**

Table 3 Performance comparison of VMC and MPC-VMC with different primal controller's tuning

	VMC		MPC-VMC	
G_m[dB]	τ_r, ms	τ_s, ms	τ_r, ms	τ_s, ms
5	0.63	1.28	**0.07**	**0.65**
10	0.72	0.91	**0.41**	**0.53**
20	2.00	2.478	**0.73**	**0.95**

controllers have been tuned. The authors tested also the effectiveness of the approach with different primal controller tunings, namely a more aggressive primal controller, and a less aggressive one. The purpose of the test is to show that, for different tunings of the primal controller, the MPC-VMC is always able to improve the performance of the standard VMC. Table 3 show this comparison for different tuning of the primal controller, changing the gain margin G_m.

Experimental results on the same DC–DC converter confirm the reliability and feasibility of the approach. Test acquisitions are collected with a Tektronix DPO3014 Digital Phosphor Oscilloscope. The primal controller and the MPC have been coded on the F28335 Delfino DSP by Texas Instruments©. The DSP belongs to C2000 series, commonly used in electrical devices control. It runs a 150 MHz unit with 32-bits architecture and IEEE-754 single-precision floating-point unit. Two control interrupts regulate the execution of the primal controller and the MPC loop. The first is executed at 400 kHz, equal to the switching frequency, whereas the MPC loop runs at 100 kHz, following the same setup of simulation test. Figs. 6 and 7 present the results for the increasing and decreasing step in the output voltage reference, respectively. The results obtained in the simulation environment have been confirmed by this experimental test. The quantitative comparison of the results is detailed in Table 4. During the positive step signal MPC-VMC guarantees a reduction of 58.86 and 59.84% of the rise time and the settling time, respectively. During the negative step, the rise time and the settling time are reduced by 45.82 and 54.95% respectively. Figs. 6 and 7 show also the inductor current which has a faster dynamics in MPC based control, but still keeping the transient peak restrained as expected.

5 Conclusions

In this paper we have considered the use of MPC to regulate a pre-compensated power converter. With this strategy it is possible to improve performance of the control without modifying the primal regulator. This aspect is helpful when it is not possible to change the primal controller, and only the reference signal can be steered. As an advantage, the outer MPC loop can run at a slower frequency with respect to the primal controller, to meet the computational constraints of the, possible low-power, board. We applied this technique to a synchronous buck DC–DC converter, controlled with the standard VMC. The simulation and experimental results show that MPC applied to the pre-compensated system is able to improve significantly the performance of the standard VMC. The

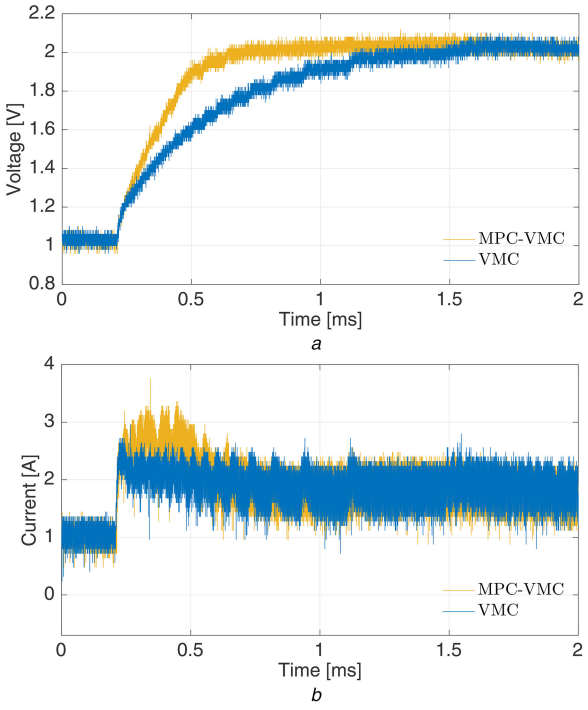

Fig. 6 *Experimental results, with an increasing output voltage step. Comparison between standard VMC and and MPC-VMC. From top to bottom: the output voltage; the inductor current*

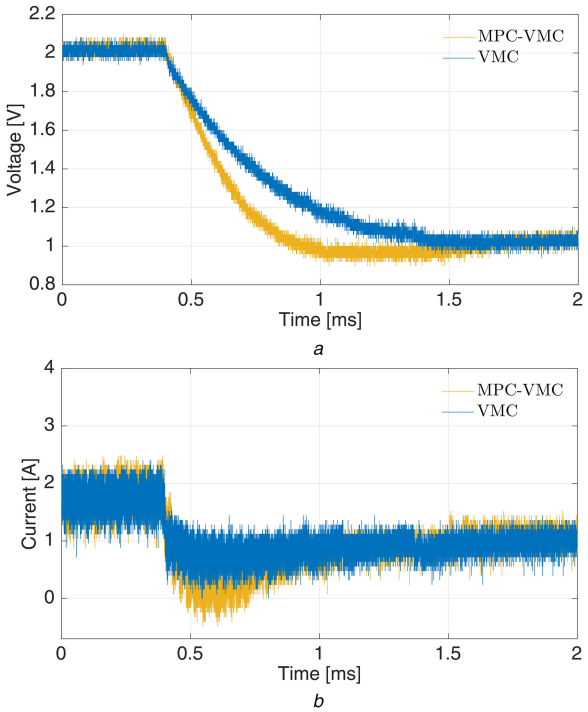

Fig. 7 *Experimental results, with a decreasing output voltage step. Comparison between standard VMC and and MPC-VMC. From top to bottom: the output voltage; the inductor current*

Table 4 Experimental improvements of MPC-VMC respect to standard VMC under step variations

		VMC	MPC-VMC
positive step	τ_r, ms	0.735	**0.3024**
	τ_s, ms	0.917	**0.3683**
negative step	τ_r, ms	0.725	**0.3928**
	τ_s, ms	0.995	**0.4482**

positive results are confirmed also with unknown load variations, and with different tunings of the primal controller. Memory allocation and computational power are marginally affected. As a future research, a constrained formulation will be investigated, with the challenge of retaining a feasible implementation in low power applications.

6 References

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